

WHAT IS CLAIMED IS:

1. A semiconductor device comprising an insulator layer having at least one of a via-hole for forming a via-stud and a trench for forming a wire on a semiconductor substrate, wherein said one of the via-stud and the wire is formed in said one of the via-hole and the trench through a barrier layer made of any one of an inorganic compound and a high melting point metal formed on inner surfaces of said one of the via-hole and the trench, said one of the via-stud and the wire being formed of the same metal as a metal composing the barrier layer.

2. A semiconductor device comprising insulator layers having a via-stud and insulator layers having a wire on a semiconductor substrate, said insulator layers having said via-stud and said insulator layers having said wire being alternately formed, wherein said via-stud and said wire are respectively formed in a via-hole and a trench through barrier layers made of any one of an inorganic compound and a high melting point metal formed on inner surfaces of the via-hole and the trench, respectively, said via-stud and said wire being formed of the same metal as a metal composing the barrier layer.

3. A semiconductor device comprising an insulator layer having at least one of a via-hole for forming a via-stud and a trench for forming a wire on a semiconductor substrate,

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wherein said one of the via-stud and the wire is formed in at least said one of the via-hole and the trench through barrier layers made of any one of an inorganic compound and a high melting point metal formed on inner surfaces of said one of the via-hole and the trench, said one of the via-stud and the wire being formed of the same metal as a metal composing the barrier layer through electroplating after electroless plating of the same metal.

4. A semiconductor device comprising an insulator layer having at least one of a via-hole for forming a via-stud and a trench for forming a wire on a semiconductor substrate, wherein said one of the via-stud and the wire is formed in said one of the via-hole and the trench through barrier layers made of any one of an inorganic compound and a high melting point metal formed on inner surfaces of said one of the via-hole and the trench, the whole of said one of the via-stud and the wire being formed through electroless plating.

5. A semiconductor device comprising insulator layers having a via-stud and insulator layers having a wire on a semiconductor substrate, said insulator layers having the via-stud and said insulator layers having the wire being alternately formed, wherein said via-stud and said wire are respectively formed in a via-hole and a trench through barrier layers made of any one of an inorganic compound and a high melting point metal formed on inner surfaces of the via-hole and the trench, respectively, said via-stud and said wire

being formed of the same metal as a metal composing the barrier layer through electroplating after electroless plating of the same metal.

6. A semiconductor device comprising insulator layers having a via-stud and insulator layers having a wire on a semiconductor substrate, said insulator layers having said via-stud and said insulator layers having said wire being alternately formed, wherein said via-stud and said wire are respectively formed in a via-hole and a trench through barrier layers made of any one of an inorganic compound and a high melting point metal formed on inner surfaces of the via-hole and the trench, respectively, an entirety of said via-stud and an entirety said wire being formed through electroless plating.

7. A semiconductor device comprising an insulator layer having a via-stud on a semiconductor substrate, wherein said via-stud is formed in a via-hole through a barrier layer made of any one of an inorganic compound and a high melting point metal formed on an inner surface of the via-hole, a diameter of said via-stud being smaller than 0.3 μm .

8. A resin sealed semiconductor device comprising a semiconductor device according to claim 7 which is sealed by a composition containing epoxy resin, spherical quartz particles and silicone polymer.

9. A resin sealed semiconductor device according to claim 8, wherein said spherical quartz particles are contained in the composition in an amount of more than 80 weight % of the total weight of said composition.

10. A module comprising a multilayer thin film wiring substrate composed of a plurality of laminated insulator layers, each of said insulator layers having a wiring layer on a surface; and a semiconductor device mounted on said wiring substrate, wherein said semiconductor device is the semiconductor device according to claim 9.

11. A large-scaled computer comprising a module substrate mounted on a printed wiring board, said module substrate being connected to said printed wiring board through connecting pins; a multilayer thin film wiring substrate mounted on said module substrate, said multilayer thin film wiring substrate having a plurality of laminated insulator layers, each of the insulator layers having a wiring layer; and the semiconductor device according to claim 9 mounted on said wiring substrate.

12. A resin sealed semiconductor device comprising a semiconductor device according to claim 1 which is sealed by a composition containing epoxy resin, spherical quartz particles and silicone polymer.

13. A resin sealed semiconductor device according to

claim 12, wherein said spherical quartz particles are contained in the composition in an amount of more than 80 weight % of the total weight of said composition.

14. A module comprising a multilayer thin film wiring substrate composed of a plurality of laminated insulator layers, each of said insulator layers having a wiring layer on a surface; and a semiconductor device mounted on said wiring substrate, wherein said semiconductor device is the semiconductor device according to claim 13.

15. A large-scaled computer comprising a module substrate mounted on a printed wiring board, said module substrate being connected to said printed wiring board through connecting pins; a multilayer thin film wiring substrate mounted on said module substrate, said multilayer thin film wiring substrate having a plurality of laminated insulator layers, each of the insulator layers having a wiring layer; and the semiconductor device according to claim 13 mounted on said wiring substrate.

16. A resin sealed semiconductor device comprising a semiconductor device according to claim 2 which is sealed by a composition containing epoxy resin, spherical quartz particles and silicone polymer.

17. A resin sealed semiconductor device comprising a semiconductor device according to claim 3 which is sealed by a

composition containing epoxy resin, spherical quartz particles and silicone polymer.

18. A resin sealed semiconductor device comprising a semiconductor device according to claim 4 which is sealed by a composition containing epoxy resin, spherical quartz particles and silicone polymer.

19. A resin sealed semiconductor device comprising a semiconductor device according to claim 5 which is sealed by a composition containing epoxy resin, spherical quartz particles and silicone polymer.

20. A resin sealed semiconductor device comprising a semiconductor device according to claim 6 which is sealed by a composition containing epoxy resin, spherical quartz particles and silicone polymer.